

Substitute for form 1449B/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)				Complete if Known	
				Application Number	10/781,334
				Filing Date	February 17, 2004
				First Named Inventor	Cameron McClintock
				Art Unit	2819
				Examiner Name	Don P. Le
Sheet	4	of	4	Attorney Docket Number	015114-052530US

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
he	77	UEDA et al. "A 3.3V ASIC for Mixed Voltage Applications With Shut Down Mode," <i>IEEE 1993 Custom Integrated Circuits Conference</i> , May 9-12, 1993, pp. 25.5.1 to 25.5.4.	
	78	VOLDMAN "ESD Protections in a Mixed Voltage Interface and Multi-Rail Disconnected Power Grid Environment in 0.50- and 0.25- μ m Channel Length CMOS Technologies," <i>EOS/ESD Symposium</i> , 1994, pp. 3.4.1 to 3.4.10.	
	79	VU et al. "A Gallium Arsenide SDFL Gate Array with On-Chip RAM," <i>IEEE Journal of Solid-State Circuits</i> , Vol. sc-19, No. 1, February 1984, pp. 10-22.	
he	80	WILLIAMS "Mixing 3-V and 5-V ICs," <i>IEEE Spectrum</i> , March 1993, pp. 40-42.	

Examiner Signature	Don P. Le	Date Considered	8/26/04
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² Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached.

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we	61	Altera Corporation, Data Sheet, "Flex 10K Embedded Programmable Logic Family," Jul., 1995, ver. 1, pp. 1-39.	
	62	Altera Corporation, Data Sheet, "Apex 20K," May, 1999, pp. 23-88.	
	63	CHAPPELL et al. "Fast CMOS ECL Receivers With 100-mV Worst-Case Sensitivity," <i>IEEE Journal of Solid-State Circuits</i> , Vol. 23, No. 1, February 1988, pp. 59-66.	
	64	CLAUDE "Cross-boundary PLDs," <i>Semiconductor Currents</i> , June 1991, pp. 9-10.	
	65	GUARDIANI et al. "Applying a submicron mismatch model to practical IC design," <i>IEEE 1994 Custom Integrated Circuits Conference</i> , 1994, pp. 297-300.	
	66	GUNNING et al., "A CMOS Low-Voltage-Swing Transmission-Line Transceiver," <i>IEEE International Solid-State Circuits Conference</i> , 1992, pp. 58-59.	
	67	HAINES "Field-programmable gate array with non-volatile configuration," <i>Microprocessors and Microsystems</i> , "Vol. 13, No. 5, June 1989, pp. 305-312.	
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	69	MARTINEZ "IEEE 1194.1 BTL-Enabling Technology for High Speed Bus Applications," National Semiconductor Application Note 829, June 1992, pp. 1-5.	
	70	KNACK "Debunking High-Speed PCB Design Myths," <i>ASIC & EDA</i> , July 1993, pp. 12-26.	
	71	PELGROM et al. "A 3/5 V Compatible I/O Buffer," <i>IEEE Journal of Solid-State Circuits</i> , Vol. 30, No. 7, July 1995, pp. 823-825.	
	72	PELGROM et al. "Matching Properties of MOS Transistors," <i>IEEE Journal of Solid-State Circuits</i> , Vol. 24, No. 5, October 1989, pp. 1433-1440.	
	73	PRINCE et al. "ICs going on a 3-V diet," <i>IEEE Spectrum</i> , May 1992, pp. 23-25.	
	74	ROBERTS et al. "Session XIX: High Density SRAMs," <i>IEEE International Solid-State Circuits Conference</i> , February 27, 1987, pp. 252-254.	
	75	SENTHINATHAN et al., "Application Specific CMOS Output Driver Circuit Design Techniques to Reduce Simultaneous Switching Noise," <i>IEEE Journal of Solid-State Circuits</i> , Vol. 28, No. 12, December 1993, pp. 1383-1388.	
me	76	SENTHINATHAN et al., "Simultaneous Switching Ground Noise Calculation for Packaged CMOS Devices," <i>IEEE Journal of Solid-State Circuits</i> , Vol. 26, No. 11, November 1991, pp. 1724-1728.	

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U.S. PATENT DOCUMENTS+						
Examiner Initials*	Cite No. ¹	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
W	42	US-4,783,607		11-08-1988	Hsieh	
	43	US-4,742,252		05-03-1988	Agrawal	
	44	US-4,625,129		11-25-1986	Ueno	
	45	US-4,527,079		07-02-1985	Thompson	
	46	US-4,472,647		09-18-1984	Allgood et al.	
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W	48	US-4,032,800		06-28-1977	Droscher et al.	

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Examiner Initials*	Cite No. ¹	Foreign Patent Document			Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Country Code ³	Number ⁴	Kind Code ⁵ (if known)				
W	49	EP	0 358 501	A2	14-03-1990	Kawasaki Steel		<input type="checkbox"/>
	50	EP	0 426 283	B1	29-12-1997	SGS Thompson		<input type="checkbox"/>
	51	EP	0750242	A2	12-27-1996	Fujitsu Ltd.		<input type="checkbox"/>
	52	EP	0718977	A2	06-26-1996	ST Microelectronics		<input type="checkbox"/>
	53	EP	0 616 431	A1	21-09-1994	AMD		<input type="checkbox"/>
W	54	EP	0 608 515	A1	03-08-1994	Motorola		<input type="checkbox"/>
	55	EP	0 544 481	A1	02-06-1993	AT&T		<input type="checkbox"/>
	56	JP	04-223617		08-13-1992	Ricoh		abstract only
	57	JP	02-161820		06-21-1990	Kawasaki		abstract only
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W	59	JP	01-274512		11-02-1989	Hitachi		abstract only
	60	PCT	WO98/47230		10-22-1998	Xilinx, Inc.		<input type="checkbox"/>

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PTO/SB/08A (08-03)

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M	1	US-6,335,637	01-01-2002	Corrales, Jr. et al.	
	2	US-6,229,365	05-08-2001	Iketani et al.	
	3	US-6,049,227	04-11-2000	Goetting et al.	
	4	US-6,040,712	03-21-2000	Mejia	
	5	US-6,018,252	01-25-2000	Imazumi	
	6	US-5,974,476	10-26-1999	Lin et al.	
	7	US-5,815,013	09-29-1998	Johnston	
	8	US-5,798,659	08-25-1998	Shay et al.	
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	10	US-5,589,783	12-31-1996	McClure	
	11	US-5,583,454	12-10-1996	Hawkins et al.	
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	37	US-4,933,577	06-12-1990	Wong et al.	
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	39	US-4,820,937	04-11-1989	Hsieh	
	40	US-4,797,583	01-10-1989	Ueno et al.	
41	US-4,791,312	12-13-1988	Weick		

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